IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of extracting circuit characteristics from a circuit design, said method comprising:

extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;

determining a difference between said first cell characteristics and said second cell characteristics; [[and]]

labeling a placeability of said portion of said circuit design based on said difference[[.]];

replacing said portion of said circuit with a leaf cell if said portion of said circuit design is freely placeable; and

merging all overlapping shapes within said leaf cell into a single shape.

2. (Original) The method in claim 1, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.

3. (Original) The method in claim 1, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.

4. (Original) The method in claim 3, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.

5. (Original) The method in claim 1, wherein said labeling of said placeability comprises:

comparing said difference to a predetermined standard; and

labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.

6. (Currently Amended) A method of extracting circuit characteristics from a circuit design, said method comprising:

extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;

determining a difference between said first cell characteristics and said second cell characteristics;

labeling a placeability of said portion of said circuit design based on said difference; [[and]]

replacing said portion of said circuit with a placeholder cell if said portion of said circuit design is freely placeable[[.]]; and

merging all overlapping shapes within said placeholder cell into a single shape.

7. (Original) The method in claim 6, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.

8. (Original) The method in claim 6, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.

9. (Original) The method in claim 8, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.

10. (Original) The method in claim 6, wherein said labeling of said placeability comprises:

comparing said difference to a predetermined standard; and

labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.

11. (Original) The method in claim 6, further comprising calculating average cell characteristics from said portion of said circuit design for said placeholder cell based on an average environment.

12. (Currently Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of

extracting circuit characteristics from a circuit design, said method comprising:

extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;

determining a difference between said first cell characteristics and said second cell characteristics; [[and]]

labeling a placeability of said portion of said circuit design based on said difference[[.]];

replacing said portion of said circuit with a leaf cell if said portion of said circuit design is freely placeable; and

merging all overlapping shapes within said leaf cell into a single shape.

13. (Original) The program storage device in claim 12, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.

14. (Original) The program storage device in claim 12, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.

15. (Original) The program storage device in claim 14, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.

16. (Original) The program storage device in claim 12, wherein said labeling of said placeability comprises:

comparing said difference to a predetermined standard; and

labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.

17. (Currently Amended) A method of extracting circuit characteristics from a circuit design, said method comprising:

extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;

determining a difference between said first cell characteristics and said second cell characteristics;

comparing said difference to a predetermined standard;

labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard;

replacing said portion of said circuit with a placeholder cell if said portion of said circuit design is freely placeable;

simplifying said placeholder cell ~~in a process comprising~~ by merging all overlapping shapes within said placeholder cell into a single shape, wherein said merging comprises:

shorting all conductors in said portion of said circuit design to a ground node;

merging all conductors in a given level of said portion of said circuit design;

removing all conductors that are covered by overlying conductors from said portion of said circuit design; and

merging conductors outside said portion of said circuit design that are within a predetermined distance to said circuit design with conductors within said portion of said circuit design.

18. (Original) The method in claim 17, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.

19. (Original) The method in claim 17, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.

20. (Original) The method in claim 19, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.

21. (Original) The method in claim 17, further comprising calculating average cell characteristics from said portion of said circuit design for said placeholder cell.